**Experiment-2 : Full Adder**

**Objective:**

To design a Single bit Full Adder and write a simple test bench for it. The test bench should generate stimulus to completely verify the functionality of the design.

**Tool Used:**

Xilinx ISE.

**Theory:**

In the case of Full Adder Circuit we have three inputs A, B and Carry In and we will get final output SUM and Carry out. So, A + B + CARRY IN = SUM and CARRY OUT.

**DUT Code:**

//Design

module fa(input a,b,c, output s,cy);

    assign s = a^b^c; //logic for sum

    assign cy = a&b | b&c | a&c; //logic for carry

endmodule

**TB Code:**

//TB

module tb();

    reg a,b,c; //inputs

    wire s,cy; //outputs

    integer x=0; //error counter

    fa dut(a,b,c,s,cy); // instantiation

    initial begin

        repeat(100) begin //100 tests

            {a,b,c} = $random; //random input stimuli

            #1; //delay to see dut output

            if ({cy,s} != a+b+c) x = x+1; // check if the output is as expected

        end

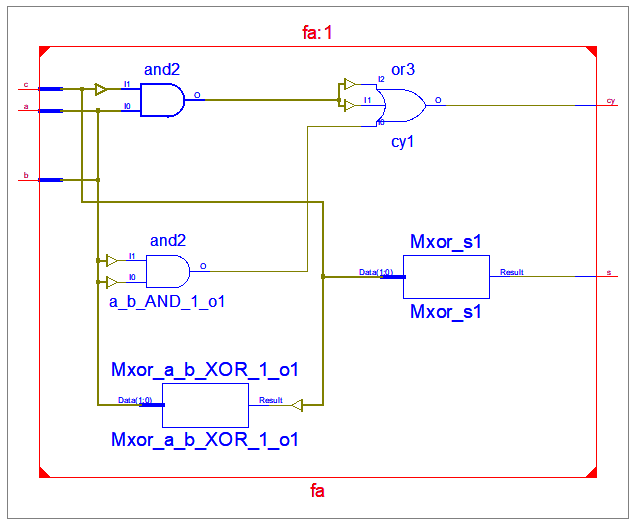
        if(!x) $display("SUCCESS"); //print success if correct

        else $display("FAILURE"); //print failure is not

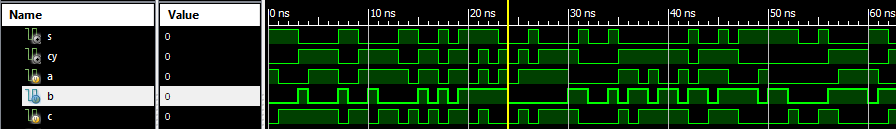
    end

endmodule

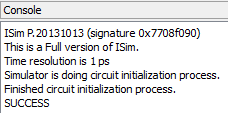
**RTL Diagram:**

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**Output Waveform:**

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**Simulation Output:**

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**Result:**

The simulation output and the RTL diagram is observed and found to be valid.